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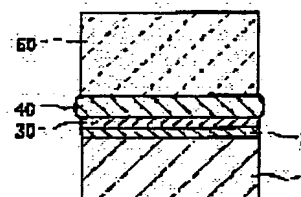
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(54) NITRIDE SEMICONDUCTOR ELEMENT AND MANUFACTURE THEREOF

(57)Abstract:

PURPOSE: To take out an electrode from the upper and the lower sides by a method wherein a conductive board is bonded to the surface of the nitride semiconductor layer of a wafer on which the nitride semiconductor layer is grown on an insulated board, and the nitride semiconductor layer is exposed by removing a part of the entire insulated board of the wafer after bonding.

CONSTITUTION: A wafer, on which a nitride semiconductor layer 2 is laminated, is prepared on the surface of a sapphire board. Then, an ohmic electrode 30 is formed on almost the whole surface of the nitride semiconductor layer 2. On the other hand, a P-type GaAs board 50, having the size almost same as the sapphire board 1, is prepared as a conductive board, and the second ohmic electrode 40 is formed on the surface of the above-mentioned board 50. Then, the ohmic electrodes of the nitride semiconductor wafer, having the first ohmic electrode 30, and a board 50, having the second ohmic electrode 40, are laminated with each other and they are pressure-bonded. Besides, the sapphire board is removed, and the nitride semiconductor layer 2 is exposed.



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CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of the nitride semiconductor device characterized by having the first process which pastes up a conductive substrate on the nitride semiconductor stratification plane of the wafer with which the nitride semiconductor layer grew on the insulating substrate, and the second process at which a part or all of the insulating substrate of the aforementioned wafer is removed, and a nitride semiconductor layer is exposed after conductive substrate adhesion.

[Claim 2] The aforementioned conductive substrate is the manufacture method of the nitride semiconductor device according to claim 1 characterized by having cleavage nature.

[Claim 3] The manufacture method of the claim 1 characterized by pasting up a nitride semiconductor stratification plan and a conductive substrate through an electrode or a conductive material in the first process of the above, or a nitride semiconductor device according to claim 2.

[Claim 4] The manufacture method of the nitride semiconductor device according to claim 3 characterized by including the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face on which the aforementioned electrode was formed in the nitride semiconductor layer front face.

[Claim 5] The nitride semiconductor device which a conductive substrate and a nitride semiconductor paste up and is characterized by the bird clapper.

[Claim 6] The nitride semiconductor device according to claim 5 characterized by the aforementioned conductive substrate having cleavage nature.

[Claim 7] The claim 5 characterized by the aforementioned conductive substrate and the aforementioned nitride semiconductor light emitting device having pasted up through an electrode or a conductive material, or a nitride semiconductor device according to claim 6.

[Claim 8] The nitride semiconductor device according to claim 7 characterized by including the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face on which the aforementioned electrode was formed in the nitride semiconductor layer front face.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the element which consists of a nitride semiconductor ($\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, $0 \leq x, 0 \leq y, x+y \leq 1$) used for light-receiving devices, such as luminescence devices, such as light emitting diode and laser diode, or a photodiode, and its manufacture method.

[0002]

[Description of the Prior Art] Since a nitride semiconductor has the bandgap energy to 1.9eV – 6.0eV, it is observed as various objects for semiconductor devices, such as a light emitting device and a photo detector, and blue Light Emitting Diode using this material and the bluish green color Light Emitting Diode were just put in practical use recently.

[0003] Generally a nitride semiconductor device is obtained using vapor growths, such as MBE and MOVPE, by carrying out laminating growth of the nitride semiconductor which specified the conductivity type to n type, p type, or i type on the substrate. Although it is known that conductive substrates, such as silicon carbide besides insulating substrates, such as sapphire, a spinel, a lithium niobate, and gallium acid neodymium, silicon, a zinc oxide, and gallium arsenide, can be used for a substrate. The substrate which carries out grid adjustment completely with a nitride semiconductor is not yet developed, but the blue which now grew up the nitride semiconductor layer compulsorily on the sapphire with which lattice constants differ 10% or more, and the bluish green color Light Emitting Diode element are put in practical use.

[0004] Drawing 6 is the typical cross section showing the structure of the conventional blue Light Emitting Diode element. The conventional Light Emitting Diode element has the structure to the double by which the laminating of n type layer 62 and the barrier layer 63 which consist of a nitride semiconductor on silicon on sapphire 61 fundamentally, and the p type layer 64 was carried out to order. As mentioned above, since sapphire is insulation and cannot take out an electrode from a substrate side, it considers as the so-called element of the flip chip method with which the positive electrode 65 and the negative electrode 66 were formed in the same nitride semiconductor layer front face.

[0005]

[Problems to be Solved by the Invention] However, there are many troubles in the element of the conventional flip chip method which uses sapphire as a substrate. Probably, in order to take out both electrodes from the same side in the first place, a chip size becomes large and much chips are not obtained from a wafer by it. Since the negative electrode and the positive electrode are horizontally located in a line, current flows horizontally, as a result, current density becomes high locally, and a chip generates heat [second]. Since a substrate which is called sapphire and which is very hard and does not have cleavage nature is used [third], advanced technology is needed for chip-izing. Since the cleavage plane of a nitride semiconductor which used the cleavage nature of a substrate is not made with a resonance side in case it is furthermore going to realize LD, formation of a resonance side is very difficult.

[0006] Although the attempt which grows a nitride semiconductor as mentioned above on conductive substrates, such as silicon carbide, silicon, a zinc oxide, gallium arsenide, and gallium phosphorus, is also accomplished in order to avoid the above problems, the report of having still succeeded is not carried out.

[0007] Therefore, this invention is accomplished in view of such a situation, and the place made into the purpose is to offer the manufacture method of the nitride semiconductor device which has the structure which can take out an electrode mainly from the upper and lower sides, and a nitride semiconductor device.

[0008]

[Means for Solving the Problem] The manufacture method of the nitride semiconductor device of this invention is characterized by having the first process which pastes up a conductive substrate on the nitride semiconductor stratification plane of the wafer with which the nitride semiconductor layer grew on the insulating substrate, and the second process at which a part or all of the insulating substrate of the aforementioned wafer is removed, and a nitride semiconductor layer is exposed after conductive substrate adhesion. Moreover, a conductive substrate and a nitride semiconductor paste up and the nitride semiconductor device of this invention is characterized by the bird clapper.

[0009] In the method of this invention, sapphire, a spinel, a lithium niobate, gallium acid neodymium, etc. are used for an insulating substrate as mentioned above, and sapphire and the nitride semiconductor which grew on the spinel are preferably excellent in crystallinity. On the other hand, if it is the substrate material which has conductivity, what thing may be used, for example, Si, SiC, GaAs, GaP and InP, ZnSe, ZnS, ZnO, etc. can be used for the conductive substrate pasted up on a nitride semiconductor. However, a conductive substrate cannot be overemphasized by choosing the substrate of the shape of a wafer which has the almost same configuration as the insulating substrate to which the laminating of the nitride semiconductor was carried out, and has a bigger area than the further almost same area or it.

[0010] On the other hand, in order to remove the insulating substrate of the wafer with which the laminating of the nitride semiconductor layer was carried out, technology, such as polish and etching, is used. Usually, there is hundreds of micrometers thickness of an insulating substrate, since a nitride semiconductor layer is 20 micrometers or less even if thick, in case polish removes a substrate, when it is hard to control *****, a rough portion may be removed by polish at first, a fine portion may be removed by etching after that, and the nitride semiconductor side need not be removed by an electrode may be exposed. Moreover, when producing the element which uses an insulator as a current constricting layer and needs it for a nitride semiconductor layer front face, for example like a laser element, it is also possible to remove only

a portion required to expose a nitride semiconductor layer by selectively etching, without removing all insulating substrates. [0011] Furthermore, the conductive substrate pasted up on a nitride semiconductor layer in the method and element of this invention is characterized by having cleavage nature. GaAs, GaP, InP, SiC, etc. can be preferably used for the conductive substrate which has this cleavage nature.

[0012] Next, the method and element of this invention are characterized by pasting up a nitride semiconductor stratification plane and a conductive substrate through an electrode or a conductive material. Even if this method uses the substrate which has cleavage nature in a conductive substrate, it is applicable similarly. Although the so-called technique of the wafer adhesion which carries out thermocompression bonding may be used for it after making these mirror planes rival in the method of pasting up by making the adhesion side and nitride semiconductor stratification plane of a conductive substrate into a mirror plane, it can paste up easily by minding an electrode or a conductive material. If conductive material is a nitride semiconductor and the material which can paste up a conductive substrate, what thing is sufficient as them, for example, they can use material, such as In, Au, a pewter, and a silver paste.

[0013] Moreover, in the aforementioned adhesion technique, it is characterized by an electrode containing the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face which were formed in the nitride semiconductor layer front face. In addition, with an ohmic electrode, it is defined as an ohmic electrode on these specifications including metals, such as the metal for thick adhesion of the thickness attached on the thin ohmic electrode and electrode of the thickness generally formed in a nitride semiconductor front face, for example, Au, In, aluminum, etc. As an ohmic electrode material formed in a nitride semiconductor layer front face, if n type layer is an adhesion side, a kind of material of aluminum, Cr(s), Ti, and In(s) which were shown in JP,5-291621,A, the electrode which made Ti especially the side which touches n type layer preferably, and the material containing Ti-aluminum shown in JP,7-45867,A can be mentioned at least. Moreover, if an adhesion side is p type layer, a kind of material of Au(s), Pt(s), Ag, and nickel which were similarly shown in JP,5-291621,A, and the electrode which made nickel especially the side which touches p type layer preferably can be mentioned at least.

[0014] A nitride semiconductor is performed, in order for p type layer to be hard to be obtained and to obtain p type layer, for example, after electron beam irradiation which is indicated by JP,3-218625,A, and thermal annealing processing which is indicated by JP,5-183189,A growing, and p type layer on the front face of the maximum is formed into low resistance. For this reason, as for the nitride semiconductor wafer, the best layer is p type layer in many cases. Then, in case this nitride semiconductor wafer and a conductive substrate are pasted up, especially the thing for which a conductive p type substrate is pasted up through the ohmic electrode formed in p type layer is desirable.

[0015] On the other hand, if for example, a conductive substrate is n type GaAs as an ohmic electrode already formed in the conductive substrate of one of the two's adhesion side, Ag-Sn, In-Sn, nickel-Sn, Au-Sn, Au-Si, Au-germanium, etc. can be used, and if it is p type GaAs, Au-Zn, Ag-Zn, Ag-In, etc. can be used. In addition, although an ohmic electrode material well-known also about SiC and Si can be used, especially the thing for which a conductive p type substrate is pasted up through the ohmic electrode of the conductive substrate as mentioned above is desirable.

[0016]

[Function] With the method and element of this invention, the conductive substrate is pasted up on the nitride semiconductor layer. That is, although the various elements from which a nitride semiconductor is obtained from a nitride semiconductor with the wafer which grew on the insulating substrate cannot but serve as flip chip form, they serve as a substrate in which a conductive substrate forms an electrode by pasting up a conductive substrate on the nitride semiconductor layer of the wafer best layer. Then, since a nitride semiconductor layer will be exposed if an insulating substrate is removed, another electrode can be formed in the exposed nitride semiconductor stratification plane, and the element with which an electrode like before was horizontally located in a line but the element which the mutual electrode countered can be produced.

[0017] Next, if the material which has cleavage nature in the conductive substrate to paste up is chosen, the nitride semiconductor which grew on the insulating substrate without cleavage nature can also divide in the shape of a chip using the cleavage nature of the pasted-up conductive substrate. For this reason, the small element of a chip size becomes is easy to be obtained, and the laser element which makes the cleavage plane of a nitride semiconductor an optical resonance side further can be produced now.

[0018] moreover, although there is also the method of a nitride semiconductor stratification plane and a conductive substrate being the technology generally called wafer adhesion, and pasting up, it is desirable in order to also stabilize the electrical property between a conductive substrate and a nitride semiconductor layer, if it pastes up through the electrode of a nitride semiconductor layer, the electrode of a conductive substrate, or a conductive material especially. When choosing the material which can furthermore reflect the luminescence wavelength of nitride semiconductors, such as Au, aluminum, and Ag, as this conductive material and a light emitting device is produced, the light which comes to the conductive substrate which such conductive material pasted up is reflected, and since there is an operation returned to a nitride semiconductor layer side, the luminous efficiency of a light emitting device improves.

[0019] If the ohmic electrode formed in the ohmic electrode and/or the conductive substrate front face which were formed in the nitride semiconductor layer front face especially as a charge of a binder is included, when a luminescence device like a light emitting device will be produced, for example, resistance becomes low and there is an operation which reduces V_f of a device.

[0020]

[Example] Hereafter, this invention is explained in full detail in the example. Drawing 1 or drawing 3 is a wafer explaining on process of the method of this invention, and the typical cross section of a conductive substrate, and drawing 4 is the typical cross section showing the structure of the nitride semiconductor light emitting device obtained according to the example 1, and describes an example 1 based on these drawings.

[0021] The nitride semiconductor layer 2 prepares for the front face of [example 1] silicon on sapphire 1 the wafer by which the laminating was carried out. In addition, the nitride semiconductor layer 2 has the structure to the double which has at least n type layer 21 which consists of $\text{AlXGa}_{1-X}\text{N}$ ($0 < X < 1$) by which the donor impurity was doped sequentially from silicon on sapphire 1, the barrier layer 22 which consists of $\text{InYGa}_{1-Y}\text{N}$ ($0 < Y < 1$), and p type layer 23 which consists of

AlXGa $1-X$ N ($0 < X < 1$) by which acceptor impurity was dop d. In addition, p type layer 23 of the best layer is formed into low resistance by annealing 400 degrees C or more.

[0022] Next, as shown in drawing 1, the ohmic electrode 30 of the front face of the nitride semiconductor layer 2 which contains nickel and Au on the whole surface is mostly formed by 500Å thickness. That is, the first ohmic electrode 30 formed on the whole surface of the nitride semiconductor layer 2 as a p type layer is obtained mostly by forming, in order, further, an ohmic electrode 30 and to improve an adhesive property, 0.1 micrometers of Au thin films are formed.

[0023] The p type GaAs substrate 50 which, on the other hand, has the almost same size as silicon on sapphire 1 as a conductive substrate is prepared, and the second ohmic electrode 40 which consists of Au-Zn is formed in the front face of this p type GaAs substrate 50 by 500Å thickness. In order to improve an adhesive property on the second ohmic electrode 40 further, 0.1 micrometers of Au thin films are formed.

[0024] Next, the ohmic electrodes of the nitride semiconductor wafer which has the first ohmic electrode 30 as shown in drawing 2, and the p type GaAs substrate 50 which has the second ohmic electrode 40 are stuck by pressure by lamination and heating. However, it is made to become parallel [the silicon on sapphire 1 of a wafer, and the p type GaAs substrate 50] at the time of sticking by pressure. It is because the level surface of the nitride semiconductor layer exposed does not come out in the process which removes the following silicon on sapphire unless it is parallel. Moreover, although Au was used in order to paste up the first ohmic electrode 30 and the second ohmic electrode 40, it is also possible to paste up through conductive material, such as an indium, tin, a pewter, and a silver paste, among electrodes 30 and 40. In addition, in case the p type GaAs substrate 50 is pasted up, doubling the direction of a cleavage with a substrate 50 with the cleavage nature of a nitride semiconductor layer, and having pasted up cannot be overemphasized.

[0025] Next, the wafer on which the p type GaAs substrate 50 was pasted up is installed in the burnisher, silicon on sapphire 1 is wrapped, silicon on sapphire is removed, and n type layer 21 of the nitride semiconductor layer 2 is exposed. In addition, after wrapping silicon on sapphire 1 so that the thickness of about several micrometers may remain, it is [in this process] also possible to remove the silicon on sapphire which remained further by etching. The structure of the wafer after silicon-on-sapphire 1 removal is shown in drawing 3.

[0026] n type layer after polishing the front face of n type layer 21 exposed at the end — ohmic one — the negative electrode 25 which consists of Ti-aluminum as an electrode of business is formed, and the positive electrode 55 which consists of Au-Zn as an ohmic electrode as well as the p type GaAs substrate 50 on the other hand is formed in the whole surface.

[0027] The wafer with which the positive electrode and the negative electrode were formed as mentioned above is divided into the luminescence chip of 200-micrometer angle using the cleavage nature of a p type GaAs substrate. The typical cross section showing the structure of the luminescence chip after separation is shown in drawing 4. By energizing between an electrode 25 and 55, this luminescence chip shows the structure of a Light Emitting Diode element where a barrier layer 22 emits light. Since it was reflected by the interface of the first ohmic electrode 30 and p type layer 23 and, as for this light emitting device, luminescence of a barrier layer 22 was not absorbed by the p type GaAs substrate 50, compared with the conventional light emitting device, the radiant power output increased 50% or more.

[0028] Moreover, although sapphire and the conductive substrate explained p type GaAs, they may use an insulating substrate like a spinel and neodymium gallate described above besides sapphire to the insulating substrate, for example, and as for this example, an insulating substrate may use a substrate like Si and ZnO for a conductive substrate.

[0029] In case silicon on sapphire 1 is wrapped in the [example 2] example 1, it wraps so that it may remain by the thickness whose silicon on sapphire 1 is 5 micrometers. Next, the mask of the configuration which can form a current constriction layer in the front face of the silicon on sapphire 1 which remained is formed, etching removes the silicon on sapphire 1 of mask opening by the etching system, and a part of n type layer 21 is exposed. A positive electrode 55 is formed in n type layer like the exposure back at a negative electrode 25 and the p type GaAs substrate 50.

[0030] Next, using the cleavage nature of the p type GaAs substrate 50, it dissociates in the shape of a chip, and considers as a laser element. Drawing 5 is the typical cross section showing the structure of the laser element, and the silicon on sapphire 1 which it left intentionally is acting as a current constriction layer of a laser element. Although this example showed the example which leaves silicon on sapphire as a current constriction layer, in addition after it all removes silicon on sapphire 1 like an example 1 to form the current constriction layer of a laser element, you may form it on the nitride semiconductor layer which exposed an insulator layer like SiO₂ and TiO₂, for example.

[0031]

[Effect of the Invention] Since the nitride semiconductor device which has a conductive substrate is realizable according to the method of this invention as explained above, the small element of a chip size can be offered. Moreover, since the electrodes formed in the element have countered, current flows uniformly in a nitride semiconductor layer, calorific value becomes small and it also becomes possible to realize a laser element. The cleavage of a nitride semiconductor becomes possible still more easily, and since the cleavage plane is made with a resonator, production of a laser element becomes easy. If a luminescence device is realized further again, since luminescence of a nitride semiconductor layer will be reflected on an electrode front face by the electrode which pasted up the nitride semiconductor layer and the conductive substrate, a radiant power output can also be increased.

[0032] As the conventional nitride semiconductor Light Emitting Diode was shown in drawing 6, the positive electrode 65 of the front face of p type layer 64 which penetrates light was mostly formed in the whole surface. This is because the current of p type layer cannot spread easily. 50% or more of the light which emits light by this positive electrode 65 was absorbed. However, according to the element of this invention, it is shown in drawing 4 and drawing 5 — as — low — since n type layer [****] 21 turns into the best layer, it becomes unnecessary to prepare a whole surface electrode like before, and is good at a small partial electrode. Therefore, the junction efficiency of the light from a nitride semiconductor layer side improves by leaps and bounds, and a radiant power output improves. Thus, when this invention realizes the device which uses the nitride semiconductor, the utility value on industry is very large.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.

[Drawing 2] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.

[Drawing 3] The type section view of the nitride semiconductor wafer explaining one process of the method of this invention.

[Drawing 4] The type section view showing the structure of the nitride semiconductor device concerning one example of this invention.

[Drawing 5] The type section view showing the structure of the nitride semiconductor device concerning other examples of this invention.

[Drawing 6] The type section view showing the structure of the conventional nitride semiconductor light emitting device.

[Description of Notations]

- 1 Silicon on sapphire
- 2 Nitride semiconductor layer
- 21 n type layer
- 22 Barrier layer
- 23 p type layer
- 30 First ohmic electrode
- 40 Second ohmic electrode
- 50 p type GaAs substrate
- 25 Negative electrode
- 55 Positive electrode

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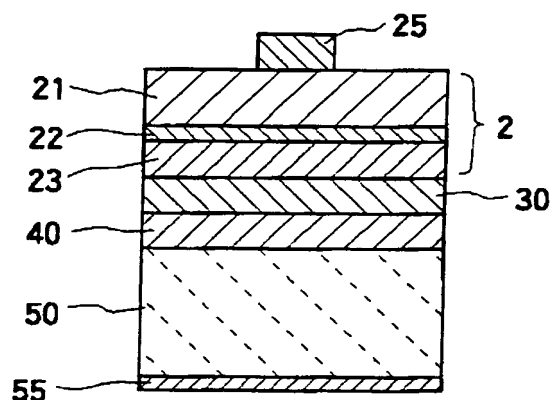
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(54) 【発明の名称】 窒化物半導体素子の製造方法及び窒化物半導体素子

(57) 【要約】

【目的】 上下より電極を取り出せる構造を有する窒化物半導体素子の製造方法、および窒化物半導体素子を提供する。

【構成】 絶縁性基板の上に窒化物半導体層が成長されたウェーハの窒化物半導体層面に導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して窒化物半導体層を露出させる第二の工程とを備え、露出させた窒化物半導体層と、導電性基板とに対向する電極を設ける。



【特許請求の範囲】

【請求項1】 絶縁性基板の上に窒化物半導体層が成長されたウェーハの窒化物半導体層面に導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して窒化物半導体層を露出させる第二の工程とを備えることを特徴とする窒化物半導体素子の製造方法。

【請求項2】 前記導電性基板は劈開性を有することを特徴とする請求項1に記載の窒化物半導体素子の製造方法。

【請求項3】 前記第一の工程において、窒化物半導体層面と導電性基板とを電極、又は導電性材料を介して接着することを特徴とする請求項1、又は請求項2に記載の窒化物半導体素子の製造方法。

【請求項4】 前記電極が窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする請求項3に記載の窒化物半導体素子の製造方法。

【請求項5】 導電性基板と窒化物半導体とが接着されてなることを特徴とする窒化物半導体素子。

【請求項6】 前記導電性基板が劈開性を有することを特徴とする請求項5に記載の窒化物半導体素子。

【請求項7】 前記導電性基板と前記窒化物半導体発光素子とが電極、又は導電性材料を介して接着されていることを特徴とする請求項5、又は請求項6に記載の窒化物半導体素子。

【請求項8】 前記電極が窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする請求項7に記載の窒化物半導体素子。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は発光ダイオード、レーザダイオード等の発光デバイス、又はフォトダイオード等の受光デバイスに使用される窒化物半導体 ($\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, $0 \leq x$, $0 \leq y$, $x+y \leq 1$) よりなる素子とその製造方法に関する。

【0002】

【従来の技術】窒化物半導体はそのバンドギャップエネルギーが $1.9 \text{ eV} \sim 6.0 \text{ eV}$ までであるので発光素子、受光素子等の各種半導体デバイス用として注目されており、最近この材料を用いた青色LED、青緑色LEDが実用化されたばかりである。

【0003】一般に窒化物半導体素子はMBE、MOVPE等の気相成長法を用いて、基板上にn型、p型あるいはi型等に導電型を規定した窒化物半導体を積層成長させることによって得られる。基板には例えばサファイア、スピネル、ニオブ酸リチウム、ガリウム酸ネオジウム等の絶縁性基板の他、炭化ケイ素、シリコン、酸化亜鉛、ガリウム砒素等の導電性基板が使用できることが知

られているが、窒化物半導体と完全に格子整合する基板は未だ開発されておらず、現在のところ、格子定数が10%以上も異なるサファイアの上に窒化物半導体層を強制的に成長させた青色、青緑色LED素子が実用化されている。

【0004】図6は従来の青色LED素子の構造を示す模式的な断面図である。従来のLED素子は、基本的にサファイア基板61の上に窒化物半導体よりなるn型層62と活性層63とp型層64とが順に積層されたダブルヘテロ構造を有している。前記のようにサファイアは絶縁性であり基板側から電極を取り出すことができないので、同一窒化物半導体層表面に正電極65と負電極66とが設けられた、いわゆるフリップチップ方式の素子とされている。

【0005】

【発明が解決しようとする課題】しかしながら、サファイアを基板とする従来のフリップチップ方式の素子には数々の問題点がある。まず第一に、同一面側から両方の電極を取り出すためチップサイズが大きくなり多数のチップがウェーハから得られない。第二に、負電極と正電極とが水平方向に並んでいるため電流が水平方向に流れ、その結果電流密度が局部的に高くなりチップが発熱する。第三にサファイアという非常に硬く、劈開性のない基板を使用しているため、チップ化するのに高度な技術が必要とする。さらにLDを実現しようとする際には基板の劈開性を用いた窒化物半導体の劈開面を共振面とできないので共振面の形成が非常に困難である。

【0006】以上のような問題を回避するため、上記のように炭化ケイ素、シリコン、酸化亜鉛、ガリウム砒素、ガリウムリン等の導電性基板の上に窒化物半導体を成長する試みも成されているが、未だ成功したという報告はされていない。

【0007】従って本発明はこのような事情を鑑み成されたものであって、その目的とするところは、主として上下より電極を取り出せる構造を有する窒化物半導体素子の製造方法、および窒化物半導体素子を提供することにある。

【0008】

【課題を解決するための手段】本発明の窒化物半導体素子の製造方法は、絶縁性基板の上に窒化物半導体層が成長されたウェーハの窒化物半導体層面に導電性基板を接着する第一の工程と、導電性基板接着後、前記ウェーハの絶縁性基板の一部、又は全部を除去して窒化物半導体層を露出させる第二の工程とを備えることを特徴とする。また、本発明の窒化物半導体素子は導電性基板と窒化物半導体とが接着されてなることを特徴とする。

【0009】本発明の方法において、絶縁性基板には前記のようにサファイア、スピネル、ニオブ酸リチウム、ガリウム酸ネオジウム等が用いられ、好ましくはサファイア、スピネルの上に成長された窒化物半導体が結晶性

に優れている。一方、窒化物半導体に接着する導電性基板には、導電性を有する基板材料であればどのようなものでも良く、例えばSi、SiC、GaAs、GaP、InP、ZnSe、ZnS、ZnO等を用いることができる。但し、導電性基板は窒化物半導体が積層された絶縁性基板とほぼ同じ形状を有し、さらにほぼ同じ面積か、あるいはそれよりも大きな面積を有するウェーハ状の基板を選択することはいうまでもない。

【0010】一方、窒化物半導体層が積層されたウェーハの絶縁性基板を除去するには、例えば研磨、エッチング等の技術を用いる。通常絶縁性基板の厚さは数百 μm あり、窒化物半導体層は厚くても20 μm 以下であるので、研磨により基板を除去する際に研磨厚が制御しにくい場合は、最初研磨で大きな部分を除去し、その後エッチングで細かい部分を除去して、電極を形成するのに必要とする窒化物半導体面を露出させても良い。また例えばレーザ素子のように絶縁物を電流狭窄層として窒化物半導体層表面に必要とする素子を作製する場合には、絶縁性基板全てを除去せずに、選択エッチングにより窒化物半導体層を露出させるのに必要な部分のみを除去することも可能である。

【0011】さらに本発明の方法及び素子において、窒化物半導体層に接着する導電性基板は劈開性を有することを特徴とする。この劈開性を有する導電性基板には、例えばGaAs、GaP、InP、SiC等を好ましく用いることができる。

【0012】次に本発明の方法及び素子は窒化物半導体層面と導電性基板とを電極、又は導電性材料を介して接着することを特徴とする。この方法は導電性基板に劈開性のある基板を使用しても同様に適用可能である。接着する方法には、導電性基板の接着面と、窒化物半導体層面とを鏡面として、それら鏡面同士を張り合わせた後、熱圧着するいわゆるウェーハ接着の手法を用いてもよいが、電極又は導電性材料を介することにより簡単に接着することができる。導電性材料は窒化物半導体と導電性基板を接着できる材料であればどのようなものでも良く、例えばIn、Au、ハンダ、銀ペースト等の材料を使用することができる。

【0013】また前記接着手法において、電極は窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含むことを特徴とする。なお、オーミック電極とは、一般に窒化物半導体表面に形成される膜厚の薄いオーミック電極と、その電極の上に付けられた膜厚の厚い接着用の金属、例えばAu、In、Al等の金属を含んで本明細書ではオーミック電極と定義する。窒化物半導体層表面に形成するオーミック電極材料としては、n型層が接着面であれば例えば特開平5-291621号公報に示されたAl、Cr、Ti、Inの内の少なくとも一種の材料、特に好ましくはTiをn型層と接する側とした電極、また

特開平7-45867号公報に示されたTi-Alを含む材料を挙げることができる。また接着面がp型層であれば同じく特開平5-291621号公報に示されたAu、Pt、Ag、Niの内の少なくとも一種の材料、特に好ましくはNiをp型層と接する側とした電極を挙げることができる。

【0014】窒化物半導体はp型層が得られにくく、p型層を得るため例えば特開平3-218625号公報に開示されるような電子線照射、また特開平5-183189号公報に開示されるような熱的アニーリング処理が成長後に行われ、最表面のp型層が低抵抗化される。このため窒化物半導体ウェーハは最上層がp型層になっていることが多い。そこで、この窒化物半導体ウェーハと導電性基板を接着する際には、p型層に形成されたオーミック電極を介してp型の導電性基板とを接着することが特に望ましい。

【0015】一方、もう片方の接着面の導電性基板に形成するオーミック電極としては例えば導電性基板がn型GaAsであれば、Ag-Sn、In-Sn、Ni-Sn、Au-Sn、Au-Si、Au-Ge等を用いることができ、p型GaAsであれば、Au-Zn、Ag-Zn、Ag-In等を用いることができる。その他SiC、Si等についても公知のオーミック電極材料を用いることができるが前記のようにp型の導電性基板をその導電性基板のオーミック電極を介して接着することが特に望ましい。

【0016】

【作用】本発明の方法及び素子では窒化物半導体層に導電性基板を接着している。つまり、窒化物半導体が絶縁性基板の上に成長されたウェーハでは、窒化物半導体より得られる各種素子はフリップチップ形式とならざるを得ないが、導電性基板をウェーハ最上層の窒化物半導体層に接着することにより、導電性基板が電極を形成する基板となる。その後、絶縁性基板を除去すると窒化物半導体層が露出するので、露出した窒化物半導体層面にもう一方の電極を形成することができ、従来のような電極が水平方向に並んだ素子ではなく、互いの電極が対向した素子を作製することができる。

【0017】次に接着する導電性基板に劈開性のある材料を選択すると、劈開性のない絶縁性基板の上に成長された窒化物半導体でも、接着された導電性基板の劈開性を利用してチップ状に分割できる。このためチップサイズの小さい素子が得られやすくなり、さらに窒化物半導体の劈開面を光共振面とするレーザ素子が作製できるようになる。

【0018】また窒化物半導体層面と導電性基板とは一般にウェーハ接着と呼ばれる技術で接着する方法もあるが、特に窒化物半導体層の電極、若しくは導電性基板の電極、又は導電性材料を介して接着すると導電性基板と窒化物半導体層との間の電気的特性も安定化するため好

ましい。さらにこの導電性材料としてAu、Al、Ag等の窒化物半導体の発光波長を反射できる材料を選択すれば、発光素子を作製した際、これらの導電性材料が接着した導電性基板に来る光を反射して、窒化物半導体層の側に戻す作用があるので発光素子の発光効率が向上する。

【0019】特に接着材料として、窒化物半導体層表面に形成されたオーミック電極及び／又は導電性基板表面に形成されたオーミック電極を含めば、例えば発光素子のような発光デバイスを作製すると、抵抗値が低くなり 10 デバイスのVfを低下させる作用がある。

【0020】

【実施例】以下、実施例で本発明を詳説する。図1乃至図3は本発明の方法の工程を説明するウェーハ及び導電性基板の模式的な断面図であり、図4は実施例1により得られた窒化物半導体発光素子の構造を示す模式的な断面図であり、以下これらの図を元に実施例1を述べる。

【0021】〔実施例1〕サファイア基板1の表面に窒化物半導体層2が積層されたウェーハを用意する。なお窒化物半導体層2はサファイア基板1から順にドナー不純物がドーパされたAlXGa1-XN ($0 \leq X \leq 1$) よりなるn型層21と、InYGa1-YN ($0 < Y < 1$) よりなる活性層22と、アクセプター不純物がドーパされたAlXGa1-XN ($0 \leq X \leq 1$) よりなるp型層23とを少なくとも有するダブルヘテロ構造を有している。なお最上層のp型層23は400℃以上のアニーリングにより低抵抗化されている。

【0022】次に図1に示すように窒化物半導体層2の表面のほぼ全面にNiとAuを含むオーミック電極30 30 を500オングストロームの膜厚で形成する。つまり窒化物半導体層2の最上層のp型層のほぼ全面にp型層と好ましいオーミックが得られる第一のオーミック電極30を形成する。さらにそのオーミック電極30の上には接着性を良くするためにAu薄膜を0.1μm形成する。

【0023】一方、導電性基板として、サファイア基板1とほぼ同じ大きさを有するp型GaAs基板50を用意し、このp型GaAs基板50の表面にAu-Znよりなる第二のオーミック電極40を500オングストロームの膜厚で形成する。さらにその第二のオーミック電極40の上に接着性を良くするためにAu薄膜を0.1μm形成する。

【0024】次に、図2に示すように第一のオーミック電極30を有する窒化物半導体ウェーハと、第二のオーミック電極40を有するp型GaAs基板50とのオーミック電極同士を貼り合わせ、加熱により圧着する。但し、圧着時ウェーハのサファイア基板1とp型GaAs基板50とは平行となるようにする。平行でないと次のサファイア基板を除去する工程において、露出される窒 50

化物半導体層の水平面が出ないからである。また第一のオーミック電極30と第二のオーミック電極40とを接着するためにAuを使用した、この他電極30と40との間にインジウム、錫、ハンダ、銀ペースト等の導電性材料を介して接着することも可能である。なおp型GaAs基板50を接着する際に窒化物半導体層の劈開性と、基板50との劈開方向を合わせて接着してあることは言うまでもない。

【0025】次にp型GaAs基板50を接着したウェーハを研磨器に設置し、サファイア基板1のラッピングを行い、サファイア基板を除去して、窒化物半導体層2のn型層21を露出させる。なおこの工程において、例えばサファイア基板1を数μm程度の厚さが残るようにラッピングした後、さらに残ったサファイア基板をエッチングにより除去することも可能である。サファイア基板1除去後のウェーハの構造を図3に示す。

【0026】最後に露出したn型層21の表面をポリシングした後、n型層にオーミック用の電極としてTi-Alよりなる負電極25を形成し、一方p型GaAs基板50には同じくオーミック電極としてAu-Znよりなる正電極55を全面に形成する。

【0027】以上のようにして正電極および負電極が形成されたウェーハを、p型GaAs基板の劈開性を利用して200μm角の発光チップに分離する。分離後の発光チップの構造を示す模式的な断面図を図4に示す。この発光チップは電極25と55間に通電することにより、活性層22が発光するLED素子の構造を示している。この発光素子は活性層22の発光が第一のオーミック電極30とp型層23との界面で反射され、p型GaAs基板50に吸収されることがないので、従来の発光素子に比べて発光出力が50%以上増大した。

【0028】またこの例は絶縁性基板がサファイア、導電性基板がp型GaAsについて説明したが、絶縁性基板にはサファイアの他に例えば前記したスピネル、ネオジムガレートのような絶縁性基板を用いても良く、また導電性基板にはSi、ZnOのような基板を用いても良い。

【0029】〔実施例2〕実施例1においてサファイア基板1をラッピングする際、サファイア基板1が5μmの膜厚で残るようにラッピングする。次に残ったサファイア基板1の表面に電流狭窄層が形成できるような形状のマスクを形成し、エッチング装置でマスク開口部のサファイア基板1をエッチングにより除去し、n型層21の一部を露出させる。露出後同様にn型層に負電極25とp型GaAs基板50に正電極55を形成する。

【0030】次にp型GaAs基板50の劈開性を用いて、チップ状に分離してレーザ素子とする。図5はそのレーザ素子の構造を示す模式的な断面図であり、故意に残したサファイア基板1がレーザ素子の電流狭窄層として作用している。この例は電流狭窄層としてサファイア

基板を残す例を示したが、この他にレーザ素子の電流狭窄層を形成するには実施例 1 のようにサファイア基板 1 を全部除去してから、例えば SiO_2 、 TiO_2 のような絶縁膜を露出した窒化物半導体層の上に形成しても良い。

【0031】

【発明の効果】以上説明したように、本発明の方法によると導電性基板を有する窒化物半導体素子可以实现できるので、チップサイズの小さい素子を提供することができる。また素子に形成した電極同士が対向しているので、電流が窒化物半導体層に均一に流れ発熱量が小さくなり、レーザ素子を実現することも可能となる。さらに容易に窒化物半導体の劈開が可能となり、その劈開面を共振器とできるためレーザ素子の作製が容易となる。さらにまた発光デバイスを実現すると、窒化物半導体層と導電性基板とを接着した電極により、窒化物半導体層の発光が電極表面で反射されるので発光出力も増大させることができる。

【0032】従来の窒化物半導体 LED は図 6 に示すように p 型層 64 の表面のほぼ全面に光を透過する正電極 65 が形成されていた。これは p 型層の電流が広がりにくいことによる。この正電極 65 により発光する光の 50% 以上が吸収されていた。しかし本発明の素子によると図 4 および図 5 に示すように低抵抗な n 型層 21 が最上層となるので、従来のように全面電極を設ける必要がなくなり、小さな部分電極でよい。従って窒化物半導体層側からの光の取り出し効率が飛躍的に向上し発光出力

が向上する。このように本発明は窒化物半導体を用いたデバイスを実現する上で産業上の利用価値は非常に大きい。

【図面の簡単な説明】

【図 1】 本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図 2】 本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図 3】 本発明の方法の一工程を説明する窒化物半導体ウェーハの模式断面図。

【図 4】 本発明の一実施例に係る窒化物半導体素子の構造を示す模式断面図。

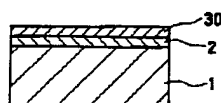
【図 5】 本発明の他の実施例に係る窒化物半導体素子の構造を示す模式断面図。

【図 6】 従来の窒化物半導体発光素子の構造を示す模式断面図。

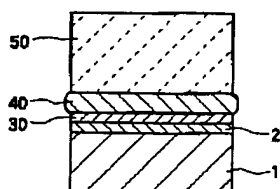
【符号の説明】

- 1・・・サファイア基板
- 2・・・窒化物半導体層
- 21・・・n 型層
- 22・・・活性層
- 23・・・p 型層
- 30・・・第一のオーミック電極
- 40・・・第二のオーミック電極
- 50・・・p 型 GaAs 基板
- 25・・・負電極
- 55・・・正電極

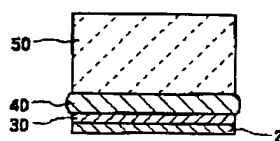
【図 1】



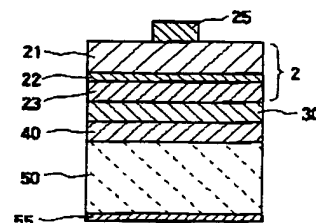
【図 2】



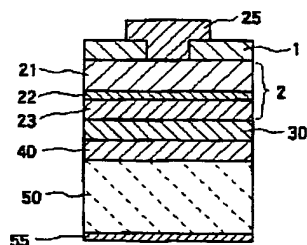
【図 3】



【図 4】



【図 5】



【図 6】

